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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,717	01/12/2004	Takehito Kobayashi	118291	1339

25944 7590 12/01/2005

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EXAMINER	
BUI, HUNG S	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,717	KOBAYASHI, TAKEHITO	
	Examiner	Art Unit	
	Hung S. Bui	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *13-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of the restriction in the reply filed on 08/17/2005 is acknowledged. The traversal is on the ground(s) that applicant states that the group of claims would encompass a search for the subject matter of the remaining claims. This is not found persuasive because the method of manufacturing a circuit board is classified in class 29 necessitating additional search and/or consideration. The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda [US 2001/0012212] in view of Wieloch et al. [US 5,835,356].

Regarding claims 1 and 4, Ikeda discloses a power circuit structural body (figures 1-2), comprising:

- at least one semiconductor switching element (11a-11f or 51);
- a power circuit (13) for outputting an inputted electric power through the semiconductor switching element (figure 1);

- a control circuit (15) for controlling drive of the semiconductor switching element (figure 1);
- a printed circuit board (31, 41) having a board body, a conductive pattern (31a, 41a) constituting the power circuit and disposed on one surface thereof, wherein the board body has at least one through-hole (31b) for mounting the semiconductor switching element thereon; and
- the semiconductor switching element is mounted to one of the conductive patterns on the printed circuit board.

Ikeda discloses the instant claimed invention except for the specific of mounting the semiconductor switching to a printed circuit board.

Wieloch et al. disclose a power substrate module having a board body including a through hole (figure 3) for mounting at least one semiconductor switching (204), wherein the at least one semiconductor switching is mounted to one of a conductive pattern (280) disposed on one side of a printed circuit board (248), and to another side of a conductive pattern (209) through a through hole (figure 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the mounting design of Wieloch et al. with the printed circuit board of Ikeda, for the purpose of saving space in the substrate module.

Regarding claim 2, Ikeda discloses the instant claimed invention except for a reinforcing plate laminated over one of the conductive patterns of the printed circuit board.

Wieloch et al. further disclose a reinforcing plate (285) laminated over one of the conductive patterns of the printed circuit board to which the semiconductor switching element being mounted thereto (figure 3, column 5, lines 15-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the reinforcing plate the printed circuit board of Ikeda, as suggested by Wieloch et al., in order to provide a strengthening of the printed circuit board.

Regarding claims 3 and 5, Ikeda, as modified, disclose the instant claimed invention except for the reinforcing plate being formed of aluminum alloy in fixed the through hole.

Official notice is taken that it is well know to use an aluminum alloy that has a light weight, good electrical and thermal conductivity, high reflectivity and resistance to oxidation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the reinforcing plate of Ikeda, as modified, to fix the though hole, in order to provide a good thermal conductivity and a less weight of the module.

Regarding claims 6-7, Weiloch et al. further disclose the reinforcing plate being fixed to heat dissipating member (292-294, figure 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the reinforcing plate with a heat member of Ikeda, as suggested by Weiloch et al., for the purpose of dissipating heat from the semiconductor switching in the power module.

Regarding claim 8, Ikeda discloses wherein a terminal for connecting the power circuit or the control circuit to an external circuit that is connected to the adequate conductive pattern on the printed circuit board.

Regarding claim 9, Ikeda further discloses a case (20) for accommodating the printed circuit board (figures 2-3) and a housing (12) disposed on the case for surrounding the terminal and constituting a connector together with the terminal.

Regarding claim 12, Ikeda further disclose a heat dissipating member for cooling the printed circuit board; wherein the printed circuit board is interposed between the heat dissipating member and the case (figures 2-3).

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda, as modified, as applied to claim 9 above, and further in view of Sumida et al. [US 5,928004].

Regarding claim 10, Ikeda, as modified, disclose the instant claimed invention except for the specific of the terminal mounted within the module.

Sumida et al. disclose an electrical connection box (figure 14) having terminals which are fixed to a printed circuit board (216) in a state in which the terminal penetrates through the printed circuit board in the direction of thickness of the printed circuit board and projects into the housing through a casing in the direction of thickness (figure 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use terminal connection design of Suminda et al. in Ikeda, as modified, for the purpose of securing and providing electrical connection.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda, as modified, as applied to claim 9 above, and further in view of Learmonth [US 6,049,468]

Regarding claim 11, Ikeda, as modified, disclose the instant claimed invention except for the specific of the casing to enclosure the printed circuit board.

Learmonth discloses a printed circuit board (14, figure 1) being enclosure of a case that is divided along the printed circuit board and the direction parallel to the printed circuit board with two halves (16, 17, figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the casing design of Learmonth in Ikeda, as modified, for the purpose of enabling installation the power assembly.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung S. Bui whose telephone number is (571) 272-2102. The examiner can normally be reached on Monday-Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11/7/05
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Art Unit 2841

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